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(FILE 'USPAT' ENTERED AT 10:04:08 ON 25 JAN 1999)  
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FILE 'JPO' ENTERED AT 10:20:54 ON 25 JAN 1999  
L1 269291 S MEMORY  
L2 2 S L1 AND AMORPHOUS (W) SILICON (W) CARBIDE  
L3 0 S L2 AND A-SIC

=> d l2 cit 1-2

1. JP360242678A , Dec. 2, 1985, SEMICONDUCTOR **MEMORY** DEVICE;  
TAKESHITA, TETSUYOSHI, et al.,  
INT-CL: H01L29/78

2. JP360184681A , Sep. 20, 1985, **AMORPHOUS SILICON CARBIDE**  
FILM FOR COATING; YAMASHITA, TAKURO, et al.,  
INT-CL: C23C16/30  
ADDITIONAL-INT-CL: C01B31/36

=> d l2 cit ab 1-2

1. JP360242678A , Dec. 2, 1985, SEMICONDUCTOR **MEMORY** DEVICE;  
TAKESHITA, TETSUYOSHI, et al.,  
INT-CL: H01L29/78

JP360242678A

L2: 1 of 2

# ABSTRACT:

PURPOSE: To obtain an amorphous nonvolatile **memory**, which has excellent holding characteristics and reproducibility and a large area and large capacitance and cost thereof is low, by using an **amorphous silicon carbide** film in place of an amorphous silicon nitride film.

CONSTITUTION: An insulating substrate 11, a lower electrode 12, an N<SP>+</SP> type 13, which is hydrogenated previously by amorphous silicon and to which phosphorus is doped to a high degree, and an N type 14 to which phosphorus is doped similarly to a low degree are formed in the order. An silicon oxide film 15 in which amorphous silicon in oxidized through plasma anodizing, etc., a film 16, which consists of a hydrogenated **amorphous silicon carbide** film and contains carbon by 35atom% or more, and an upper electrode 17 are shaped in the order. Accordingly, a device having performance, which has not exist as nonvolatile memories, such as, a holding time of ten years or more, a

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L1 245964 S MEMORY  
L2 4927 S FLOATING GATE  
L3 4410 S L1 AND L2  
L4 1 S L3 AND AMORPHOUS (W) SILICON (W) CARBIDE  
L5 21 S L3 AND A-SIC  
L6 20 S L5 AND (INSULAT? OR DIELECTRIC?)

=> d 14 cit

1. 5,738,731, Apr. 14, 1998, Photovoltaic device; Masahiro Shindo, et al., 136/249, 260, 262; 257/184, 440 [IMAGE AVAILABLE]

=> d 16 cit 1-20

1. 5,828,080, Oct. 27, 1998, Oxide thin film, electronic device substrate and electronic device; Yoshihiko Yano, et al., 257/43, 310, 314, 410, 411 [IMAGE AVAILABLE]

2. 5,810,923, Sep. 22, 1998, Method for forming oxide thin film and the treatment of silicon substrate; Yoshihiko Yano, et al., 117/84, 89, 94; 427/248.1, 250 [IMAGE AVAILABLE]

3. 5,767,549, Jun. 16, 1998, SOI CMOS structure; Wei Chen, et al., 257/347, 351 [IMAGE AVAILABLE]

4. 5,766,968, Jun. 16, 1998, Micro mask comprising agglomerated material; Michael Armacost, et al., 438/398; 148/DIG.105; 204/192.15; 438/700, 964 [IMAGE AVAILABLE]

5. 5,738,731, Apr. 14, 1998, Photovoltaic device; Masahiro Shindo, et al., 136/249, 260, 262; 257/184, 440 [IMAGE AVAILABLE]

6. 5,691,209, Nov. 25, 1997, Lattice interconnect method and apparatus for manufacturing multi-chip modules; Janusz B. Liberowski, 438/10, 131 [IMAGE AVAILABLE]

7. 5,687,112, Nov. 11, 1997, Multibit single cell memory element having tapered contact; Stanford R. Ovshinsky, 365/163; 257/3, 4 [IMAGE AVAILABLE]

8. 5,623,160, Apr. 22, 1997, Signal-routing or interconnect substrate, structure and apparatus; Janusz B. Liberowski, 257/621, 50, 209, 513, 529, 530, 661, 665, 700, 758, 774; 505/220 [IMAGE AVAILABLE]

9. 5,604,357, Feb. 18, 1997, Semiconductor nonvolatile **memory** with resonance tunneling; Kashi Hori, 257/24, 25, 68, 1, 324, 410, 411 [IMAGE AVAILABLE] *Take*

*Take* 10. 5,596,522, Jan. 21, 1997, Homogeneous compositions of microcrystalline semiconductor material, semiconductor devices and directly overwritable **memory** elements fabricated therefrom, and arrays fabricated from the **memory** elements; Stanford R. Ovshinsky, et al., 365/113; 257/3, 4; 365/163 [IMAGE AVAILABLE]

11. 5,536,947, Jul. 16, 1996, Electrically erasable, directly overwritable, multibit single cell **memory** element and arrays fabricated therefrom; Patrick K. Klersy, et al., 257/3, 2, 5 [IMAGE AVAILABLE] *Take*

12. 5,534,711, Jul. 9, 1996, Electrically erasable, directly overwritable, multibit single cell **memory** elements and arrays fabricated therefrom; Stanford R. Ovshinsky, et al., 257/3, 2, 5 [IMAGE AVAILABLE]

13. 5,466,626, Nov. 14, 1995, Micro mask comprising agglomerated material; Michael Armacost, et al., 438/700; 148/DIG.105; 438/396, 947, 964 [IMAGE AVAILABLE] *fun*

14. 5,465,249, Nov. 7, 1995, Nonvolatile random access **memory** device having transistor and capacitor made in silicon carbide substrate; James A. Cooper, Jr., et al., 365/149; 257/77; 365/177, 180 [IMAGE AVAILABLE]

15. 5,406,509, Apr. 11, 1995, Electrically erasable, directly overwritable, multibit single cell **memory** elements and arrays fabricated therefrom; Stanford R. Ovshinsky, et al., 365/113; 257/3; 365/163 [IMAGE AVAILABLE]

16. 5,381,540, Jan. 10, 1995, Interface: interrupt masking with logical sum and product options; Matthew K. Adams, et al., 395/869; 364/DIG.1; 395/310, 734, 735 [IMAGE AVAILABLE]

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*Take* 18. 4,769,686, Sep. 6, 1988, Semiconductor device; Masatada Horiuchi, et al., 257/373, 384, 404 [IMAGE AVAILABLE]

*Take* 19. 4,507,673, Mar. 26, 1985, Semiconductor **memory** device; Masaharu Aoyama, et al., 257/324, 77 [IMAGE AVAILABLE]

20. 4,426,764, Jan. 24, 1984, Semiconductor **memory** device with peripheral circuits; Yasunobu Kosa, et al., 438/257; 257/316; 438/258, 261 [IMAGE AVAILABLE]